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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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In re application of: CATABAY et al.

Attorney Docket No.:  
01-471/1D / LSI1P172D1

Application No.: Filed Herewith

Examiner: Unassigned

Filed: Herewith

Group: Unassigned

Title: MULTI-STEP PROCESS FOR FORMING  
A BARRIER FILM FOR USE IN COPPER LAYER  
FORMATION

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**CERTIFICATE OF EXPRESS MAILING**

I hereby certify that this paper and the documents and/or fees referred to as attached therein are being deposited with the United States Postal Service on February 3, 2004 in an envelope as "Express Mail Post Office to Addressee" service under 37 CFR §1.10, Mailing Label Number **ER562285933US**, addressed to: Mail Stop Patent Application, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

  
Sue Funchess

**INFORMATION DISCLOSURE STATEMENT  
37 CFR §§1.56 AND 1.97(b)**

Mail Stop Patent Application  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Dear Sir:


The references listed in the attached PTO Form 1449 may be material to examination of the above-identified patent application. Applicants submit the list of these references in compliance with their duty of disclosure pursuant to 37 CFR §§1.56 and 1.97. The Examiner is requested to make these references of official record in this application. The above-identified application is a divisional application of prior application U.S. Patent Application No. 10/035,704. This prior application is being relied upon for an earlier filing date under 35 U.S.C. § 120. Because the listed references were either cited by the PTO, or submitted to the PTO in the prior application, under 37 CFR § 1.98(d) Applicants submit that copies need not be provided.

This Information Disclosure Statement is not to be construed as a representation that a search has been made, that additional information material to the examination of this application does not exist, or that these references indeed constitute prior art.

This Information Disclosure Statement is: (i) filed within three (3) months of the filing date of the above-referenced application, (ii) believed to be filed before the mailing date of a first Office Action on the merits, or (iii) believed to be filed before the mailing of a first Office Action after the filing of a Request for Continued Examination under §1.114. Accordingly, it is believed that no fees are due in connection with the filing of this Information Disclosure Statement. However, if it is determined that any fees are due, the Commissioner is hereby authorized to charge such fees to Deposit Account 12-2252 (Order No. 01-471/1D).

Respectfully submitted,

BEYER WEAVER & THOMAS, LLP

A handwritten signature in black ink, appearing to read "F. T. Kalinski II", with a stylized flourish at the end.

Francis T. Kalinski II

Registration No. 44,177

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Berkeley, CA 94704-0778

<b>Form 1449 (Modified)</b>  <b>Information Disclosure Statement By Applicant</b>  (Use Several Sheets if Necessary)	Atty Docket No.	Application No.:
	<b>01-471/1D / LSI1P172D1</b>	<b>Filed Herewith</b>
	Applicant:	
	<b>CATABAY et al.</b>	
	Filing Date	Group
	<b>Herewith</b>	<b>Unassigned</b>

#### U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
	A	5,925,415	07/20/99	Fry et al.	427	304	03/09/98
	B	6,010,962	01/04/00	Liu et al.	438	687	02/12/99
	C	6,015,749	01/18/00	Liu et al.	438	628	05/04/98
	D	6,022,808	02/08/00	Nogami et al.	438	694	03/16/98
	E	6,037,258	03/14/00	Liu et al.	438	687	05/07/99
	F	6,042,889	03/28/00	Ballard et al.	427	305	02/28/94
	G	6,066,892	05/23/00	Ding et al.	257	751	05/14/98
	H	6,162,727	12/19/00	Schonauer et al.	438	687	11/25/98
	I	6,235,406	05/22/01	Uzoh	428	620	07/13/00

#### Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation	
							Yes	No
	J							
	K							
	L							
	M							
	N							

#### Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	O	Wolfe, et al., Silicon Processing for the VLSI Era, Vol. 1 – Process Technology, 2 <sup>nd</sup> Ed., Lattice Press: Sunset Beach, CA, 2000, pp. 791-795.
	P	U.S. Patent Application No. 10/035,705, “Electroless Deposition of Copper to Form Copper Interconnect Structures”, filed 10/18/01.
	Q	
Examiner		Date Considered

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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	<b>Herewith</b>	<b>Unassigned</b>

#### U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
	AA	6,255,192B1	07/03/01	Dornisch	438	430	09/09/98
	BB	6,268,291B1	07/31/01	Andricacos et al.	438	694	12/03/98
	CC	6,287,968B1	09/11/01	Yu et al.	438	675	01/04/99
	DD	6,297,158B1	10/02/01	Liu et al.	438	687	05/31/00
	EE	6,328,871B1	12/11/01	Ding et al.	205	183	08/16/99
	FF	6,368,967B1	04/09/02	Besser	438	687	05/04/00
	GG	6,376,370B1	04/23/02	Farrar	438	678	01/18/00
	HH	6,391,777B1	05/21/02	Chen et al.	438	687	05/02/01
	II	6,429,121B1	08/06/02	Hopper et al.	438	686	02/07/01

#### Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation	
							Yes	No
	JJ							
	KK							
	LL							
	MM							
	NN							

#### Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	OO	
	PP	
	QQ	
Examiner		Date Considered

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	<b>Herewith</b>	<b>Unassigned</b>

#### U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
	AAA	6,440,849B1	08/27/02	Merchant et al.	438	658	10/18/99
	BBB	6,445,070B1	09/03/02	Wang et al.	257	751	01/29/01
	CCC	6,461,675B2	10/08/02	Paranjpe et al.	427	250	07/10/98
	DDD	6,465,376B2	10/15/02	Uzoh et al.	438	927	08/18/99
	EEE						
	FFF						
	GGG						
	HHH						
	III						

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							Yes	No
	JJJ							
	KKK							
	LLL							
	MMM							
	NNN							

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